Serial No. 10/075,726
Art Unit: 1743
Applicants' Response to the Office Action dated May 25, 2005

Amendments to the Claims

Please amend claims 1, 6, 7, 18, 19 and 20 as shown in the listing of claims below. The amendments add no new matter. This listing of claims is a complete listing of all claims ever presented in the application and replaces all prior versions, and listings, of the claims in the instant application:

Listing of Claims:

Claim 1 (Currently amended): A chip reactor comprising a carrier having at least two different forms of microreaction channels, each of the channels comprising at least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation ~~independent~~ independently of the other.

Claim 2 (Original): The chip reactor according to claim 1, wherein the carrier comprises a silicon/glass composite.

Claim 3 (Original): The chip reactor according to claim 2, wherein at least a portion of the channels is etched.

Claim 4 (Original): The chip reactor according to claim 2, wherein at least a portion of the at least one reaction space is coated with silicon dioxide.

Claim 5 (Original): The chip reactor according to claim 4, wherein the silicon dioxide has a thickness of from 50 to 2000 nm.

Claim 6 (Currently amended): The chip reactor according to claim 1, wherein the carrier has from 2 to 100 different forms of microreaction channels, each of the channels comprising at least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation ~~independent~~ independently of the other.

Claim 7 (Currently amended): The chip reactor according to claim[[,]] 1, wherein each of the reaction spaces comprises a channel having a length of from 1 to 500 mm.

Claim 8 (Original): The chip reactor according to claim 1, wherein the reaction spaces have one or more mixing points.

Claim 9 (Original): The chip reactor according to claim 1, wherein at least one of the channels has at least two inlets, the at least two inlets impinging on each other at a mixing angle of from 15° to 270°.

Claim 10 (Original): The chip reactor according to claim 1, wherein at least one of the reaction spaces has one or more mixing points.

Claim 11 (Original): The chip reactor according to claim 1, wherein the chip reactor is divided into two or more zones for variable processing.

Claim 12 (Original): The chip reactor according to claim 11, wherein the two or more zones can be heated/cooled independently of one another.

Claim 13 (Original): The chip reactor according to claim 1, wherein the carrier is embedded in a manifold having an inbound passageway corresponding to the at least one inlet and an outbound passageway corresponding to the at least one outlet.

Claim 14 (Original): The chip reactor according to claim 13, wherein the manifold comprises an inert material.

Claim 15 (Original): The chip reactor according to claim 13, wherein the manifold further comprises at least one passageway for a heat transfer liquid.

Claim 16 (Original): The chip reactor according to claim 13, wherein the manifold further comprises a facility for visual inspection of the chip reactor.

Claim 17 (Original): The chip reactor according to claim 13, further comprising a seal separating the chip reactor from the manifold.

Claim 18 (Currently amended): The chip reactor according to claim 1, wherein the carrier has at least three different forms of microreaction channels, each of the channels comprising at least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation ~~independent~~ independently of the other.

Claim 19 (Currently amended): The chip reactor according to claim 1, wherein the carrier has from 5 to 50 different forms of microreaction channels, each of the channels comprising at least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation ~~independent~~ independently of the other.

Claim 20 (Currently amended): A chip reactor comprising a silicon/glass composite carrier having from 5 to 50 different forms of microreaction channels etched therein, each of the channels comprising at least one reaction space, a portion of which is coated with silicon dioxide having a thickness of from 50 to 2000 nm, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation ~~independent~~ independently of the other, and wherein the carrier is embedded in an inert manifold having an inbound passageway corresponding to each inlet, an outbound passageway corresponding to each outlet, at least one passageway for a heat transfer liquid and a facility for visual inspection of the chip reactor.